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Attorneys for Defendant and Counterclaimant
FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation; and ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C 07-2664 JSW)

DECLARATION OF DR. RICHARD A. BLANCHARD IN SUPPORT OF FAIRCHILD'S OPENING CLAIM CONSTRUCTION BRIEF

Date: June 4, 2008
Time: 2:00 p.m.
Courtroom: Hon. Jeffrey S. White

I, Dr. Richard A. Blanchard, declare as follows:

Biography

1. I have been retained as an expert regarding semiconductor technology by Defendant and Counterclaimant Fairchild Semiconductor Corporation ("Fairchild"). This Declaration is submitted in support of Fairchild's Opening Claim Construction Brief ("Opening Brief"). I have personal knowledge of the matters stated herein and if called to testify as a witness, I could and would competently testify thereto.

2. I received a BSEE degree in 1968 and an MSEE degree in 1970 from MIT, and a PhD in Electrical Engineering from Stanford University in 1982. I was an Associate Professor, Assistant Division Chairman of the Engineering & Technology Division at Foothill College from 1974 to 1978, where among other things, I developed the curriculum for the Semiconductor Technology Program.

3. I have over 35 years of experience in the semiconductor and electronics industries. I am an exclusive expert at the Silicon Valley Expert Witness Group, Inc. ("SVEWG") and have extensive consulting experience since 1998 for SVEGW. Prior to working for SVEWG, I was Principal Engineer and Division Manager of the Electrical/Electronic Division of Failure Analysis (Exponent) Associates, Inc., from 1991 to 1998. As Division Manager, my duties included failure analysis and reverse engineering of solid-state electronic components and circuits, failure analysis of electric and electronic systems, subsystems, and components, and consulting with respect to Power MOS and Smart Power Technologies. Prior to that, I was employed by IXYS Corporation from 1987-1991, by Siliconix, Inc., from 1982-1987, by Supertex, Inc., from 1976-1982, by Cognition, Inc., from 1976 to 1978, by Foothill College from 1974-1978, as an independent consultant to the semiconductor industry from 1974-1976 and by Fairchild Semiconductor from 1970-1974.

4. I have testified in court and in deposition on numerous occasions as an expert witness, and I have served as a court-appointed special master. I have published several books and numerous articles on semiconductor design and process development, as well as failure analysis. I hold more than 130 U.S. patents on semiconductor technology. I am a member of the IEEE, the Electrostatic Discharge Society, and the International Microcircuits and Packaging Society, and the Electron Device Failure Analysis Society (EDFAS).

Task

5. I was retained by the law firm of Townsend and Townsend and Crew LLP ("Townsend"), counsel to Fairchild, to assist in this litigation. I was asked by Townsend to review the following U.S. Patents: 6,429,481 ("the '481 patent"), 6,522,497 ("the '497 patent"), 6,710,406 ("the '406 patent"), 6,828,195 ("the '195 patent"), 7,148,111 ("the '111 patent"), and 6,818,947 ("the '947 patent"). Collectively, I refer to these patents as the Fairchild Patents. Further, I refer to the '481 patent, '497 patent, '406 patent, '195 patent, and '111 patent collectively as the "Fairchild Mo Patents" since Brian Sze-Ki Mo is the first named inventor. I was asked to provide expert opinion testimony that would assist the Court in determining the meaning of the claim terms of the Fairchild Patents.

Methodology

6. The first step in the course of my analysis was to read the Fairchild Patents. I then reviewed their file histories, including the cited prior art. At times, I also reviewed the extrinsic evidence cited by the parties, including relevant sections of dictionaries and technical books from the 1997 time frame for the Fairchild Mo Patents, and from the 2002 time frame for the '947 Patent, as well as both earlier and later, to confirm the ordinary meaning of some of the terms.

7. I also reviewed the Joint Claim Construction And Pre-Hearing Statement ("the Joint Statement") that was filed on February 8, 2008. In Exhibit B of the Joint Statement, both parties present their proposed definitions for the claim terms, as well as the intrinsic and extrinsic evidence that the parties rely on in support of their respective definitions. I also used this document to consider and analyze the proposed claim constructions of the parties.

Claim Meaning

8. In determining the meaning of the claims, I relied principally on the patents themselves, their file histories, the prior art cited in the patents, and the ordinary meaning of the claim terms at the time of the effective filing date of the patent applications. My analysis was done from the perspective of a person of ordinary skill in the art of the patents at the time of the filing of the applications for the Fairchild Patents, which is shown on the face of the patents as November 1997 for the Fairchild Mo Patents and September 2002 for the '947 Patent.

9. I have reviewed Exhibit A of the Joint Statement, which sets forth the terms for which

the parties have agreed on a construction. I reviewed and analyzed those interpretations, and, based on my analysis, I concur that a person of ordinary skill in the art would interpret those terms as set forth in Exhibit A. I will not address the construction of these terms in this declaration.

10. I have reviewed Exhibit B of the Joint Statement, which sets forth the terms for which the parties have not agreed on a construction. I have analyzed each party's interpretation and support for the meanings of these disputed terms. I disagree with the proposed claim constructions offered in that document by Plaintiffs and Counterdefendants Alpha & Omega Semiconductor, Ltd., and Alpha & Omega Semiconductor, Inc. (collectively, "AOS"). Based upon my analysis and my understanding of how the term or limitation would be interpreted by a person of ordinary skill in the art at the time of the invention, I have determined that the claim constructions set forth by Fairchild are the correct interpretations.

Field Of The Fairchild Patents

11. Since the invention of the transistor half a century ago, miniaturized devices made of semiconductor materials have fueled a revolution in electronics. This case involves an important class of semiconductor transistor devices called power MOSFETs (metal oxide semiconductor field effect transistors), which are primarily used in the power supplies of electronic devices such as mobile phones, personal computers, etc. They are also used in industrial applications requiring management of high power, such as ballasts for lighting.

12. Power MOSFETs constitute a class of "field effect" transistors that are especially well adapted for use as low resistance switching devices for controlling the flow of electrical current. Field effect transistors take advantage of the inherent properties of semiconductor materials. Silicon and other semiconductor materials are useful in the field of electronics because their electrical properties can be controlled. Pure silicon is a poor conductor of electricity, but silicon becomes electrically conductive if certain impurities are added to the crystal structure.

13. The process of adding impurities into a semiconductor material is called "doping," and the impurities that are added are called "dopants." Added dopants can be either "P" type or "N" type, depending on whether they create a surplus of electrons (N-type) or a surplus of "holes" (P-type) in the semiconductor material ("P" stands for positive and "N" stands for negative). Typical materials

used for doping silicon include boron and aluminum (P-type), and arsenic and phosphorus (N-type). Heavily doped semiconductors may be referred to as P+ or N+, while lightly doped semiconductors may be referred to as P- or N-. It is common to refer to doped semiconductors as having a "conductivity type." There are only two conductivity types: P and N.

14. Silicon is the most commonly used semiconductor material, and it is employed in most types of semiconductor devices, including power MOSFETs. Silicon has excellent properties for most applications and is abundant. As a result, silicon-based processing equipment and technology have become highly advanced, such that it is generally easier to design and manufacture semiconductor devices out of silicon. Silicon is not, however, the only semiconductor material used to manufacture power MOSFETs. Other semiconductor materials, such as Silicon Carbide (SiC), are becoming more prevalent as processing technology continues to advance.

15. Power MOSFETs can be categorized as being either "lateral" or "vertical" devices. Lateral devices are those in which current flows between "source regions" and a "drain," each being located near the upper surface of the device. Vertical devices are those in which current flows between source regions near the upper surface of the device and a drain region at the bottom of the device (i.e., current flows vertically through the device). Power MOSFETs can also be categorized as being either "planar" or "trench" devices. Planar devices are those in which the gate is formed at the top surface of the device. Trench devices are those in which the gate is formed in a trench that extends into the body of the device. Figures 1 and 2 both show a cross-section of a portion of a vertical power MOSFET.

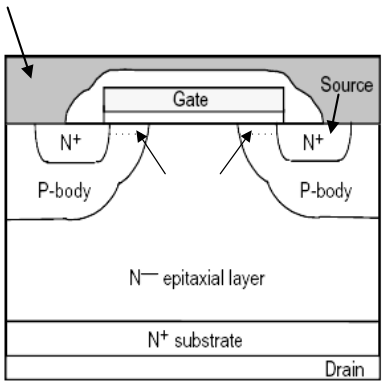

Figure 1

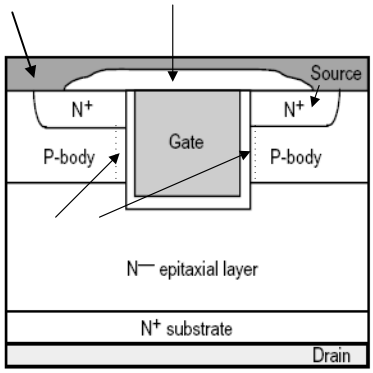

Figure 2

Figure 1 shows a cross-section of a ***planar*** vertical power MOSFET, whereas Figure 2 shows a cross-section of a ***trench*** vertical power MOSFET. As can be seen in Figures 1 and 2, the source metal is located near the top surface and the drain is located near the bottom surface. Therefore, when the device is turned on, current will flow between the top and the bottom of the device. While figures 1 and 2 depict "N-channel" devices (i.e., N source, P well, N drain), MOSFETs can also have an opposite "P-channel" arrangement of conductivity types (i.e., P source, N well, P drain). The focus of this litigation concerns vertical trench power MOSFET devices, some of which are N-channel devices and others which are P-channel devices.

16. In a power MOSFET, as in other field effect transistors, current flow between the source and the drain is controlled by the presence or absence of an electric field in a portion of the P-well, sometimes called the "body region." In the absence of a voltage applied to the gate, electrical current cannot usually flow between the source (made of N+ semiconductor material) and the drain of the device because of the presence of the P-body between the source and the drain.[1] This is because holes outnumber electrons throughout the P-body and thus there are no excess electrons available to carry current between the source and the drain. However, applying a voltage to the gate creates an electric field around the gate extending into the adjacent portion of the body region. This electric field, in turn, attracts electrons in the P-body towards the gate, creating "channel regions" in the body region where electrons outnumber holes, thus allowing current to flow from the source to the drain through the channels. Applying an appropriate voltage to the gate turns the device "on." Essentially, the conductivity type of the channel region is inverted by the presence of a sufficiently high voltage on the gate. In effect, the channel links the source and the drain with a region of the same conductivity type so that current can flow between them.

17. Most or all of the power MOSFETs involved in this litigation consist of a single transistor having a large number of source regions, one interconnected gate region, and one drain.

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[1] Under certain conditions, even if no voltage is applied to the gate, current may flow between the source and the drain, a phenomenon known as "breakdown," which is an undesirable mode of operation that I describe in more detail below.

Typical power MOSFETs usually have an array of substantially identical structures, sometimes called "cells," evenly distributed over the "active area" of the device. Actual devices may include thousands of cells formed on each die. Cells can have a variety of shapes, as can be seen from the top down view of Figures 3 and 4.

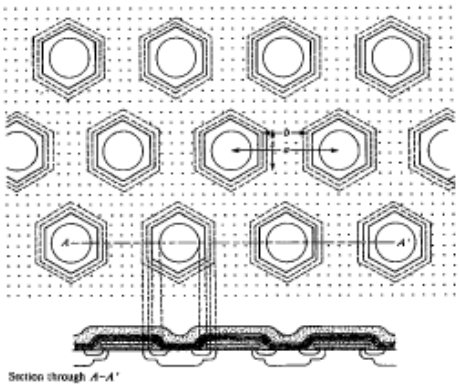

Figure 3

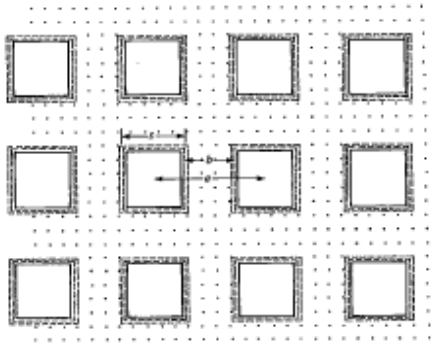

Figure 4

Figure 3 shows a power MOSFET having hexagonal-shaped cells. Figure 4, on the other hand, shows a power MOSFET having square-shaped cells. Alternatively, the cells can be arranged in a linear or striped pattern, as is shown in the figures of the Fairchild Patents.

18. The MOSFET devices of figures 1 and 2 are formed on pre-doped silicon wafers (referred to in the figures as the "N+ substrate"). A doped silicon "epitaxial" (or "epi") layer is formed on top of the wafer.[2] Some or all of the upper portion of the epitaxial layer is then converted to the opposite conductivity type (e.g., from N to P), thereby creating a P well (referred to in the figures as a "P-body"). This conversion is accomplished by adding dopants of the opposite conductivity type by ion implantation. Source regions are formed in the well by ion implantation through a mask which allows precise control of the position and shape of the sources regions. Gate structures are also formed, typically of polysilicon.[3]

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[2] "Epitaxial" means that the layer is grown as a single crystalline structure matching the crystalline structure of the wafer.

[3] The processing sequence for forming the MOSFET structures described herein may vary. For example, in the device of figure 1, the gates are formed prior to creation of the body regions, such that the presence of the gate structures prevent ion implantation of the epitaxial layer below them. Hence,

Continued on the next page

19. In the device of figure 1, the gate is formed on top of the device and is insulated from the body and epitaxial layers. In the device of figure 2, the gates are formed in trenches that are etched into the epitaxial layer and lined with an insulator such as silicon dioxide, such that the gate is also insulated from the surrounding structures. In either case, the gates themselves are made of a conductive material, usually highly doped "polysilicon" (or "poly").[4] Finally, electrical connection is made to the various structures: a metal contact layer is deposited on the bottom of the wafer connecting to the drain, and another metal layer is deposited on the top of the device for contacting the source areas. Gate contacts are not shown in the figures; typically connection is made at one or a few locations near the device periphery.

20. The fabrication of silicon-based semiconductor devices, including power MOSFETs, starts with a pre-doped silicon "wafer," sometimes referred to as a "substrate."[5] Intricate structures are formed on the wafer using various precision techniques for depositing, doping, etching, annealing, polishing and patterning materials on the wafer.[6] Typically, multiple (e.g., hundreds of) devices are

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Continued from the previous page

in figure 1 there is no body region immediately below the gate structure.

[4] More precisely, polysilicon is "polycrystalline silicon," *i.e.*, it is pure silicon consisting of a large number of randomly oriented microscopic crystal grains – as opposed to the single crystal silicon structures of the wafer and epitaxial layer.

[5] In the semiconductor field, the term "substrate" sometimes refers only to the wafer itself, and sometimes refers to the wafer and any additional layers formed on top of it. While this is occasionally confusing, which of the meanings applies is usually clear from the context.

[6] Processes for forming (*e.g.*, depositing) thin films of material on a substrate include chemical vapor deposition ("CVD") and physical vapor deposition ("PVD"). In some instances a layer of new material may be created from an existing layer – for example, the upper surface of a silicon layer can be converted to silicon dioxide – an insulating material – by heating it in the presence of oxygen. Processes for doping semiconductors include ion implantation and diffusion. Processes for etching include "wet" processes using liquid etchants (*e.g.*, acid solutions) or "dry" processes using gaseous materials (*e.g.*, plasma etching). The process for annealing involves heating the substrate to cure crystalline defects and relieve stress. Processes for patterning include photolithography to create a patterned layer, typically using a photoresist (*i.e.*, a photosensitive polymer that is deposited on the wafer and exposed through a "reticule" or "photomask" and "developed" leaving a patterned photoresist layer. Material is added to the top surface of the wafer (as by a deposition process) and selectively removed (by an etching process) using the mask layer, which is itself removed after the desired pattern has been created.

simultaneously fabricated on a single wafer, which may be as large as twelve inches (300mm) in diameter. When device fabrication is completed, the wafer is “diced” or “singulated” into individual devices, each called a “chip” or a “die.” The chips are then mounted on "die pads," connected to "leads" via "bonding wires," and encapsulated in a “package.” In a typical vertical power MOSFET, electrical connection to the gate is made via one lead, electrical connection is made to the source region via all of the remaining leads, and electrical connection to the drain is made via the die pad. The leads and a portion of the die pad extend outside of the package so that the device can be electrically connected to external circuitry.

21. Power MOSFETs combine the important goals of: (1) low on-resistance (the resistance through the device when it is turned on) to minimize power loss through the device; (2) high switching speed (the speed at which the device turns on and off) to reduce power loss during switching; (3) the ability to withstand high reverse voltages to protect attached circuitry and avoid damage to the device; and (4) high current density (the amount of current that can flow through the device at a given time) allowing the device to be made smaller and at a lower cost.

Fairchild Mo Patents

22. The Fairchild Mo Patents relate to trench power MOSFETs. As mentioned above, a power MOSFET device with a trench gate design includes one or more gates formed in trenches that are etched vertically into an underlying material. When a trench device is turned on by applying a voltage to the gate, current flows vertically through the channel that is formed adjacent to the vertical sides of the gate. A representative embodiment from the patents is set forth below:

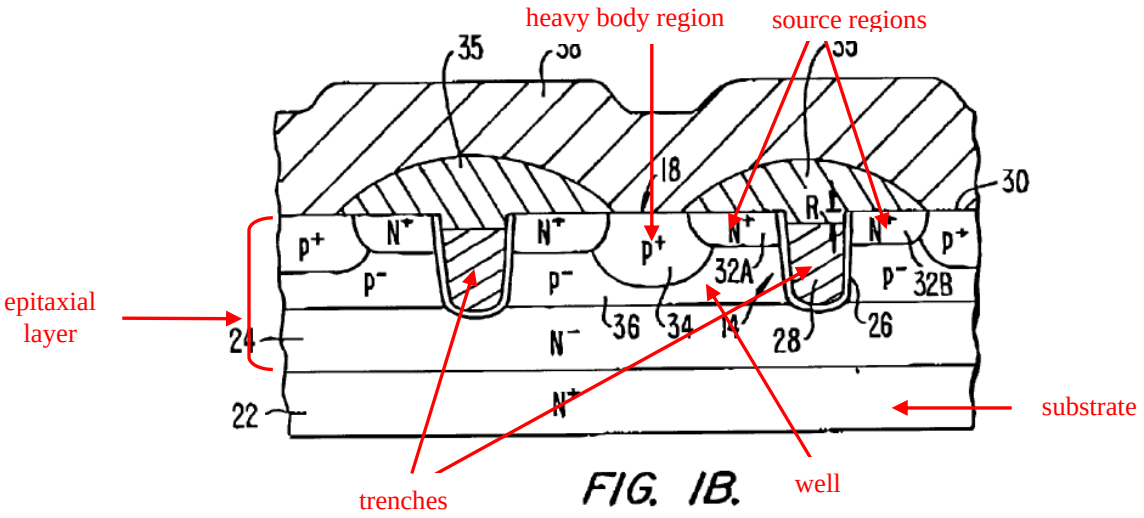


FIG. 1B.

('481 patent, Fig. 1B (annotated).) As shown in this drawing, the power MOSFET includes a substrate on which an epitaxial layer is formed. It further includes a doped well formed in the epitaxial layer, and a more heavily doped heavy body region formed in the well. Additionally, the power MOSFET includes trenches filled with a conductive material (usually polysilicon) which form gate electrodes. Source regions are formed on each side of each trench.

23. The Fairchild Mo Patents claim a novel way of controlling the phenomenon of breakdown in the active area of power MOSFETs. I briefly referred to the concept of breakdown earlier. This is an unwanted effect where current flows between the source and the drain even if no voltage is applied to the gate, i.e., the device is "on" when it should be "off." Generally, current can only flow easily in one direction across a P-N junction formed in a semiconductor device. This occurs when the P-N junction has voltage applied across it in the forward direction. If, however, the polarity of the voltage is reversed across the junction, current will not flow unless the voltage is increased to the point that current carriers are actually ripped from their locations in the silicon. This generally unwanted effect is aptly named "avalanche breakdown." The reverse voltage at which a power MOSFET will experience avalanche breakdown is referred to as its "breakdown voltage."

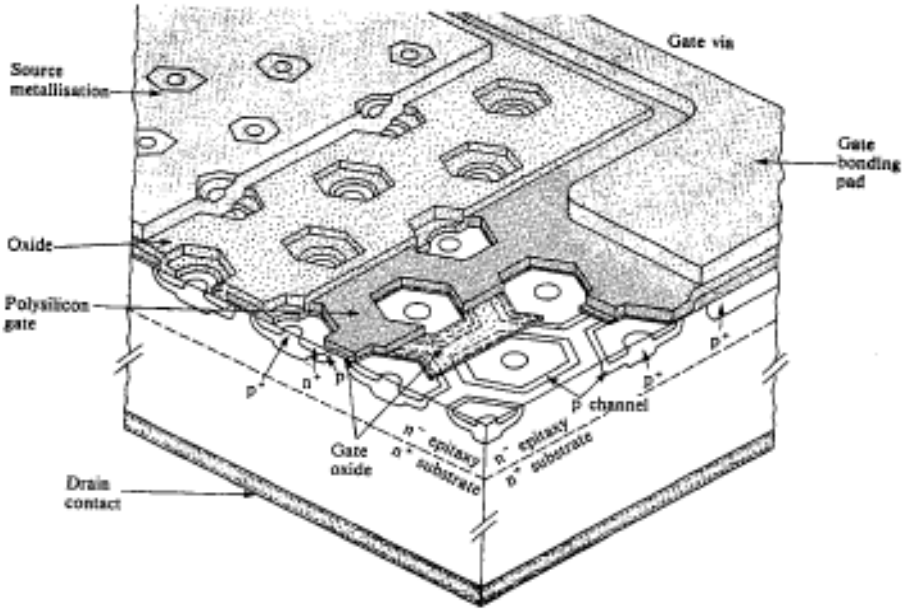
24. Power MOSFET designers go to great lengths to control breakdown because it can irreversibly damage the device. The Fairchild Mo Patents address the important goal of avoiding having the device go into breakdown near the more fragile gate structure formed in the trenches. If breakdown occurs near the gate, the thin gate oxide can be damaged. The Fairchild Mo Patents claim

a novel method and design for forming a heavy body region in the well which serves to insure that breakdown current is spaced away from the trenches. If the breakdown current is spaced away from the trenches, the device will have a much better chance of surviving the breakdown event, a characteristic that is referred to as "ruggedness." By enhancing power MOSFET ruggedness, the Fairchild Mo Patents achieve an important goal of power MOSFET design.

'947 Patent

25. The '947 patent is also directed to trench power MOSFETs. It also addresses a way of controlling the breakdown voltage of the device; however, it is directed to controlling the mechanism of breakdown in the periphery, or "termination region," of the device as opposed to the active area.

26. In a vertical power MOSFET, such as the devices at issue in this litigation, current flows through the device between the top surface and the bottom surface. Contact with the drain is made on the bottom surface of the device, and contact with the source is made on the top surface of the device above the cells in the active area. Contact with the gate is usually made in the periphery of the device, typically in one corner of the periphery. An example of a typical power MOSFET is shown in the following illustration.



This illustration shows a vertical planar power MOSFET. The device is vertical because current flows through the device between the top and bottom surfaces, and it is planar because the gate structures are

formed above the top surface of the silicon substrate. As can be seen in this illustration, there are numerous hexagonal-shaped "cells" arranged throughout the active area of the device. There is, however, only one gate, which forms an interconnected matrix of conductive material near the top surface of the device. The illustration shows that the "source metallization" covers nearly the entire active area of the device – as it has to, since the only place to contact the numerous separate cells is from above. Therefore, contact with the gate typically is made at the periphery of the device, usually on one corner. In the device shown in the illustration, contact with the gate would be made at the "gate bonding pad."

27. Since the conductive gate structure must be distributed throughout a relatively large active area, but is contacted only at only one corner in the termination region of the device, there may be a delay between the time when a voltage is applied to the gate electrode, and the time when the voltage is realized at every cell located within the active area. This delay is caused by the inherent electrical resistance that is present in all electrically conductive structures. The delay decreases the switching speed of the device. The switching speed is the speed at which the device can be switched from the "off" state to the "on" state, or *vice versa*.

28. In order to better distribute the voltage throughout the gate in the active region, a conductive ring is often formed around the perimeter of the device. This conductive ring is sometimes called a "gate runner." The gate runner has less electrical resistance than the portion that distributes the applied gate voltage to the gates in the active region. The gate runner is connected to the gate around the periphery of the active region.

29. The periphery of the chip that surrounds the active area comprises a "termination region" near the edges of the chip. The termination region can contain the gate runner and other structures that are formed to improve the performance of the device. At the time of the '947 patent, there were several techniques for increasing breakdown voltage in the termination region. Three of those techniques described in the '947 patent were field rings, field plates, and trenched field plates. One of the drawbacks of using one or more of these techniques is that they take up space in the termination region, essentially increasing the amount of space on the die that must be dedicated to edge termination structures and taking away space from the active area. This has the negative effect

of decreasing the current per unit area of the device.

30. The '947 patent addresses the problems described above by integrating a trenched gate runner and a trenched field plate into a single structure. This advancement offered the significant improvement of decreasing the amount of space that had to be dedicated to edge termination structures, while simultaneously addressing the issues of switching speed and breakdown voltage.

Level Of Ordinary Skill In The Art Of The Fairchild Patents

31. In my opinion, the Fairchild Patents were addressed to a person with at least a bachelor's degree in electrical engineering or solid-state physics and having approximately three to five years of experience in the field of power semiconductor device design, or alternatively at least a master's degree in electrical engineering or solid-state physics and one to three years of experience in the same field. This person would readily understand the design of power semiconductor devices having trenched gates, and the formation of termination structures, as well as the affects that variations in the design of such structures have on the performance characteristics of the device. The person of ordinary skill would have the requisite knowledge that I described in the "Field Of The Fairchild Patents" section above.

DISPUTED TERMS

32. In this section, I analyze and give my explanation and support for what I believe is a correct interpretation of the disputed terms and limitations of the Fairchild Patents.

WHEREIN THE HEAVY BODY FORMS AN ABRUPT JUNCTION WITH THE WELL

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
wherein the heavy body forms an abrupt junction with the well wherein the doped heavy body . . . forms an abrupt junction with the well	'481 Patent, claims 1, 6, and 15; '406 Patent, claims 1 and 13; '195 Patent, claims 1 and 21	the transition between the heavy body and well occurs over a short distance relative to the depth of the well	the doping concentration gradient at the junction between the heavy body and the well is sufficiently high that further increasing the doping concentration gradient does not further reduce the breakdown voltage at the p-n junction between the well and the substrate

33. I understand the parties dispute the meaning of the term "wherein the heavy body forms

an abrupt junction with the well" and similar language, as set forth above. For the reasons explained below, a person of ordinary skill in the art would understand "wherein the heavy body forms an abrupt junction with the well" (and variations thereof) to mean that "the transition between the heavy body and well occurs over a short distance relative to the depth of the well."

34. In the power MOSFET field, a "junction" is an interface between two regions in the device. The regions can have different characteristics, such as a heavily doped region and a less-heavily doped region, or a region containing P-type dopants and one containing N-type dopants. In simple terms, the junction is the interface at which the device changes from one region to the other. The change can be gradual or abrupt. As an analogy, the transition from a street to a sidewalk can be abrupt if the there is a curb separating the two, or gradual if there is a ramp instead of the curb.

35. Similarly, in the power MOSFET field, a junction may also be gradual or "abrupt." In the context of the patents-in-suit, a person of ordinary skill in the art would understand that an "abrupt junction" between a heavy body and a well is a transition that occurs over a short distance relative to the depth of the well. The specifications of the Fairchild Mo Patents use the term "abrupt junction" in this manner. The '481 patent, for example, describes Figure 5 of the patent as showing an abrupt junction. ('481 patent, col. 7, lines 18-38.) Figure 5 shows a “doping profile,” which is a measure of the concentration of dopants as a function of depth measured from the surface and down into the device:

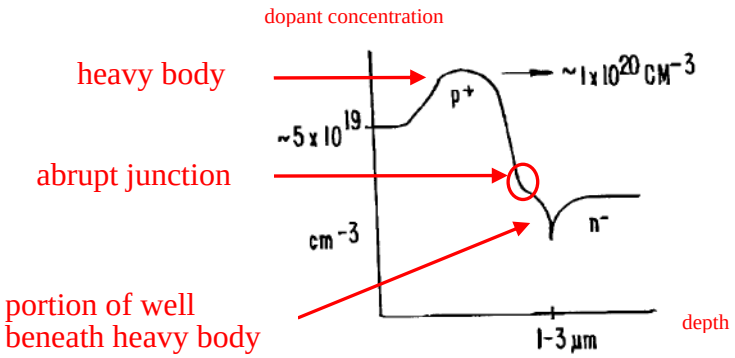


FIG. 5.

The vertical axis in this figure shows the dopant concentration in the device. The highest dopant concentration is at the top of the vertical line. The horizontal axis shows the depth into the device, as

measured from the top surface. The greatest depth is at the far right end of the horizontal axis. The "P+" region in the figure reflects the heavy body region. The figure shows an abrupt junction because the transition from the heavy body to the well occurs over a short distance. The dopant concentration (the curved black line) for the heavy body is relatively steep before the transition to the dopant concentration of the well, and there is an abrupt change in slope over a short distance where the transition occurs.

36. The file histories of the Fairchild Mo Patents describe an "abrupt junction" in the context of the patents-in-suit in the same way. During prosecution, Fairchild pointed to Figure 5 and noted that it showed the transition between the heavy body and the well "changes rapidly in a short further depth" to form the abrupt junction:

> The unique concentration profile of the p+ heavy body with respect to the p- well is depicted graphically in Fig. 5. Notice that the peak p+ heavy body is at a predetermined depth in the p- well and ***changes rapidly in a short further depth (i.e. has a steep doping concentration gradient) to form the abrupt transition with the p- well.***

('481 file history, Preliminary Amendment dated September 5, 2000, p. 8 (emphasis added).) This confirms that a person of ordinary skill in the art would understand that the term "wherein the heavy body forms an abrupt junction with the well" means "the transition between the heavy body and well occurs over a short distance relative to the depth of the well."

37. I understand that AOS proposes that this term be construed to mean "the doping concentration gradient at the junction between the heavy body and the well is sufficiently high that further increasing the doping concentration gradient does not further reduce the breakdown voltage at the p-n junction between the well and the substrate." I disagree. AOS's proposed construction is incorrect and vague in the context of the patents-in-suit.

38. It is unclear what is a "sufficiently high" gradient in AOS's proposed construction. AOS proposes that the claim language require a "sufficiently high" gradient at the junction between the heavy body and the well. The specifications of the Fairchild Mo Patents, however, do not disclose a single gradient at the junction. Instead, they teach that there are at least two gradients at the junction with a transition between them:

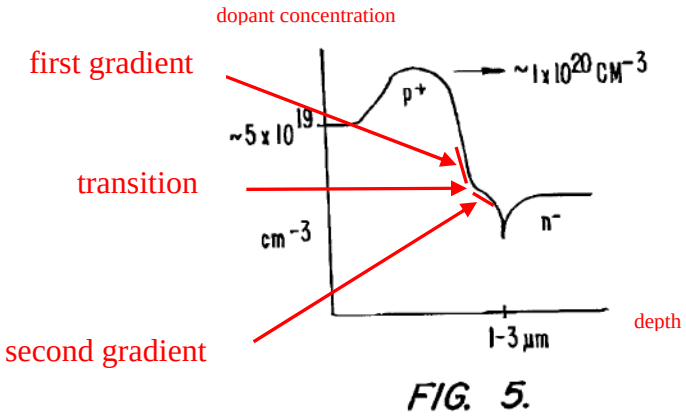


FIG. 5.

In fact, because the abrupt junction is an area of transition, there is a constantly-changing gradient in the vicinity of the abrupt junction, resulting in many different gradients on each side of the abrupt junction. Accordingly, the reference to a single gradient in AOS's proposed construction makes no sense, since it is not consistent with what is physically happening.

39. Even if one were to accept AOS's proposal that the "abrupt junction" relates to a single gradient, its proposed construction would be unclear. AOS apparently contends that an abrupt junction is present when the gradient or slope of the doping concentration profile is sufficiently steep. This construction would be unclear to a person of ordinary skill in the art because there is nothing in the specifications of the Fairchild Mo Patents, nor in their file histories, which discloses a single gradient (or slope) of the doping concentration profile for an abrupt junction. AOS's proposed construction is also flawed because there is no support in the specifications or file histories for the requirement in AOS's proposed construction that "further increasing the doping concentration gradient does not further reduce the breakdown voltage at the p-n junction between the well and the substrate." AOS's construction is also flawed because they contend an "abrupt junction" is not a "linearly graded junction," but fail to explain how they interpret "linearly graded junction." For these reasons, I disagree with AOS's proposed construction.

RESULTING IN AVALANCHE CURRENT THAT IS SUBSTANTIALLY UNIFORMLY DISTRIBUTED

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
resulting in avalanche current that is substantially uniformly distributed	'111 Patent, claim 29	resulting in avalanche current that is approximately evenly distributed across the active region of the device	the avalanche current at breakdown initiation is roughly equally distributed across the entire device

40. I understand the parties dispute the meaning of the term "resulting in avalanche current that is substantially uniformly distributed." This term appears in claim 29 of the '111 patent. For the reasons set forth below, a person of ordinary skill in the art would understand "resulting in avalanche current that is substantially uniformly distributed" to mean "resulting in avalanche current that is approximately evenly distributed across the active region of the device."

41. Power MOSFETs include several structures, including an active region where transistors are formed, a termination region in the periphery of the chip that surrounds the active region, and packaging to protect the device and permit contact with other electrical devices. The active region includes trenches, doped wells, heavy body regions, source regions, and other structures which form the transistors of the claimed invention. The current that is controlled by the power MOSFET flows through the active region. Figure 1B of the '111 patent shows a cross-sectional view of the structures of the active region:

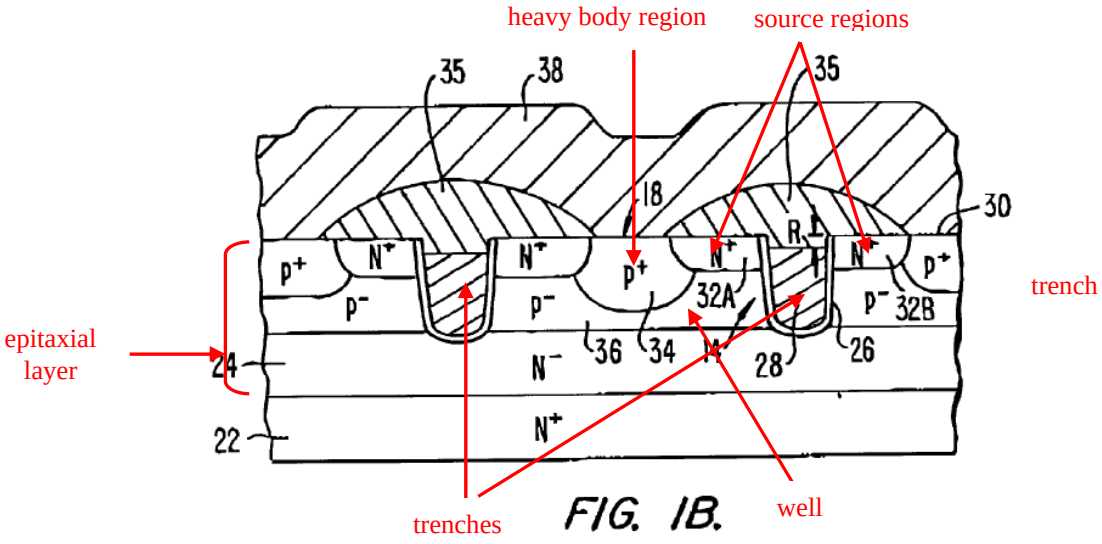


FIG. 1B.

('111 patent, Fig. 1B.) The figure shows transistor cells including trenches, a doped well, and heavy body regions formed in the doped well. The active region usually includes thousands of cells with a configuration similar to the one shown above.

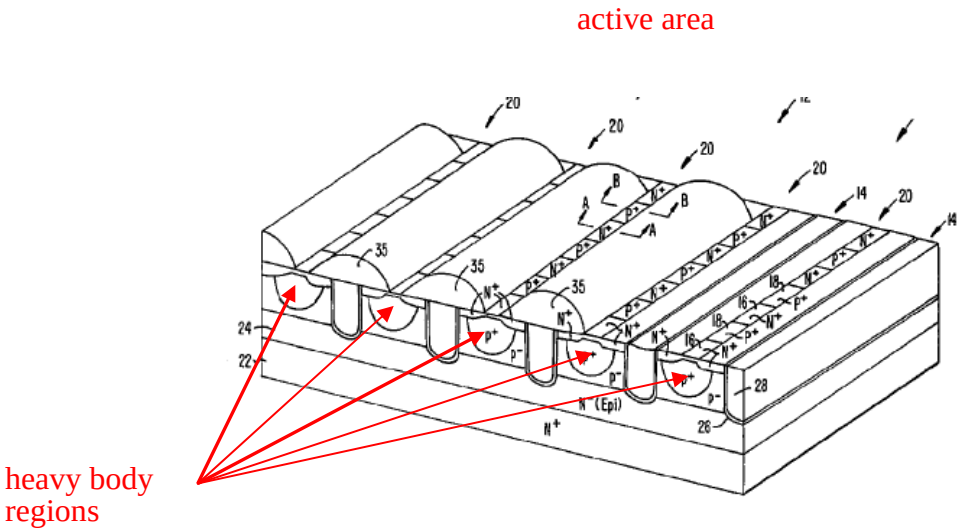
42. Claim 29 of the '111 patent relates to a method of manufacturing trench transistors, which are in the active region. Claim 29 states:

> A method of manufacturing a trench transistor comprising:
>
> providing a semiconductor substrate having dopants of a first conductivity type, the semiconductor substrate including a first highly doped drain layer and a second more lightly and substantially uniformly doped ***epitaxial layer*** atop and adjacent the first layer;
>
> forming a plurality of ***trenches*** extending to a first depth into the ***epitaxial layer***, the plurality of trenches creating a respective plurality of epitaxial mesas;
>
> lining each of the plurality of ***trenches*** with a gate dielectric material; substantially filling each dielectric-lined trench with conductive material;
>
> forming a plurality of doped ***wells*** in the plurality of epitaxial mesas, respectively to a second depth that is less than said first depth of the plurality of trenches, the plurality of doped wells having dopants of a second conductivity type opposite to said first conductivity type;
>
> forming a plurality of ***source regions*** adjacent the plurality of trenches and inside the plurality of doped wells, the source regions having a third depth and dopants of the first conductivity type;
>
> forming a plurality of ***heavy body regions*** each inside a respective one of the plurality of doped ***wells***, each heavy body region having a fourth depth between the third depth of the source region and the second depth of the doped well, and having dopants of the second conductivity type; and
>
> adjusting a dopant profile of the plurality of ***heavy body regions*** so that peak electric field is moved away from a nearby ***trench*** toward the ***heavy body*** resulting in ***avalanche current*** that is substantially uniformly distributed.

As shown above, each limitation of claim 29 relates to the formation of structures which are part of the active region, including the trench, heavy body, well, and source regions. The claimed invention also requires "avalanche current" that is "substantially uniformly distributed." As I discussed above, avalanche current flows when the device enters an undesirable condition known as "breakdown." This condition may occur when a sufficiently high voltage is applied to the device between the drain and

source which causes current to flow across P-N junctions in the reverse direction. This current is the "avalanche current" at issue in claim 29.

43. A person of ordinary skill in the art would understand that claim 29 requires the uniformity of the avalanche current to be measured in the active region of the device, i.e., where the trenches, heavy body regions, wells, source regions, and other structures of the transistors are formed. This is because it is the location of the heavy body regions between the trenches (and spaced apart from the trenches) that causes the peak electric field likewise to be located away from the trenches.



('111 patent, Fig. 1.) The figure above shows an embodiment of part of the active region and the locations of the heavy body regions in the active region. The claimed invention causes the peak electric field to be centrally located beneath each heavy body region, which is located between adjacent trenches in the figure. The location of the peak electric field, in turn, is where the avalanche current initially flows. ('111 patent, col. 5, lines 24-27 ("Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away form the sensitive gate oxide and channel regions.")) The cell design described above is the same across all of the cells in the active region. Consequently, the peak electric field where avalanche current will flow is spaced away from the trenches in every cell of the device, which are located in the active region. Because the peak electric field is approximately uniformly distributed in the active region (by being located at roughly the same location between each pair of adjacent trenches), the avalanche current also becomes

approximately evenly distributed because it flows in the same locations as the peak electric field. This results in the avalanche current being "substantially uniformly distributed" wherever it is located in the active region. The figure above illustrates this feature of the claimed invention.

44. I understand that AOS contends the claim language requires the avalanche current to be "substantially uniformly distributed" *across the entire device*. Because the "entire device" would include the termination region, I disagree. As discussed above, the active region is the only part of the device which is relevant to this claim. AOS's position would require measurement of the avalanche current in portions of the device which are unrelated to active region, including the termination region. The termination region is designed to have a higher breakdown voltage than the rest of the device, so that breakdown initiation will occur in the active area and not in the termination region.[7] The termination region surrounds the active region, but it does not contain any transistor cells. In other words, the termination region does not contain the trenches, heavy body regions, wells, and source regions which form the transistor cells. Figure 2 of the specifications of the Fairchild Mo Patents shows a cross-sectional view of an embodiment of the termination region:

[7] To optimize ruggedness, power MOSFETs are typically designed so that breakdown will occur in the active region rather than in the termination region. In other words the breakdown voltage in the termination region is designed to be higher than the breakdown voltage in the active region. Heat, which can damage the device, is generated by the flow of breakdown current through the device. The active region is relatively much larger in comparison to the termination region. If breakdown occurs, it is better if the breakdown current flows through as large an area as possible, as this will distribute the heat and thereby reduce the possibility of damage to the device. Furthermore, the active region includes more metal, further improving the ability of the active region to dissipate the heat created by the breakdown current . Therefore, optimal performance is achieved if the device is designed such that breakdown current flows throughout the active region.

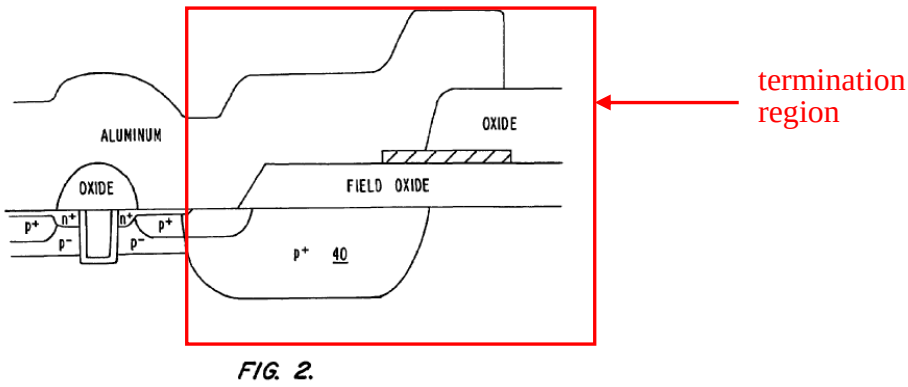


FIG. 2.

('111 patent, Fig. 2.) As shown in the above embodiment, the termination region does not contain any transistor cells, but rather includes a field termination junction (item 40), field oxide, and oxide. Because the claimed invention is directed to improving the location and distribution of the avalanche current within the cell array, as explained above, a person of ordinary skill in the art would understand the presence of any avalanche current in the termination region is outside the scope of the claimed invention.

45. I further understand that AOS contends this term requires one to measure the uniformity of the avalanche current "at breakdown initiation." A person of ordinary skill in the art would not understand this requirement to be part of the claimed invention. The claim language does not specify a particular point in time at which the avalanche current must be measured. Moreover, there is nothing in the claim language requiring the measurement to occur specifically "at breakdown initiation." When breakdown initiates in a device, avalanche current will generally begin to flow at one location in the active region and then rapidly spreads to other cells in the device. Consequently, a person of ordinary skill in the art would find the requirement urged by AOS that avalanche current be equally distributed over the entire device when the avalanche current *initiates* to be illogical.

DEPTH OF THE JUNCTION, RELATIVE TO THE DEPTH OF THE WELL, IS *ADJUSTED* SO THAT A TRANSISTOR BREAKDOWN INITIATION POINT IS SPACED AWAY FROM THE TRENCH IN THE SEMICONDUCTOR WHEN THE VOLTAGE IS APPLIED TO THE TRANSISTOR

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
depth of the junction, relative to the depth of the well, is ***adjusted*** so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor when voltage is applied to the transistor a location of the abrupt junction relative to the depth of the well is ***adjusted*** so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor depth of the heavy body relative to a depth of the well is ***adjusted*** so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor depth of the heavy body junction relative to a maximum depth of the well, is ***adjusted*** so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor	'481 Patent, claims 1, 6, and 15; '406 Patent, claims 1 and 13	Fairchild does not believe construction of this term is required. The ordinary meaning should apply.	selecting by repeated experiments or by computer simulation the relative depths of the well and the junction for the purpose of moving initiation of breakdown in the device toward the center of the body region between adjacent trenches

46. I understand the parties dispute the meaning of the term "depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor when voltage is applied to the transistor." This term appears in claim 1 of the '481 patent, and similar language appears in claims 6 and 15 of the '481 patent, as well as in claims 1 and 13 of the '406 patent. For the reasons set forth below, a person of ordinary skill in the art would understand that the ordinary meaning of this claim language should apply.

47. This term is straightforward. It requires that the depth of a structure relative to the depth of another structure (the depth of the junction relative to the depth of the well, in the context of claim 1 of the '481 patent) must be "adjusted." A person of ordinary skill in the art would understand the ordinary meaning of "adjusted" should apply. The Fairchild Mo Patents and their file histories do not state or suggest that anything other than the ordinary meaning of "adjusted" should be used. Rather, the file histories confirm that the ordinary meaning applies. When the patentees added the term "adjusted" to the claim language, for example, they made clear that the claimed invention relates to a structure in which the relative depths of the heavy body and well are "adjusted." ('481 file history, Amendment dated June 7, 2001 at 9). This is consistent with the ordinary meaning of "adjust," i.e., to change or to bring into a proper relationship. The patentees used the term "adjusted" in the same manner in another portion of the file history. ('481 file history, Amendment dated December 31, 2001 at p. 6 ("[The cited reference] Hshieh '543 expressly teaches to use a 'buried layer 16' to relocate the breakdown initiation point (col. 3, lines 3-5), and does not do so by *adjusting* the relative depths of the P+ and the well regions.")(emphasis added)). Second, this term requires that the adjustment take place such that a specific result occurs, namely "so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor when voltage is applied to the transistor." This means that the transistor breakdown initiation point cannot be located at the trench where it might cause damage, but must instead be "spaced away" from it. This is the ordinary meaning of the claim language and is consistent with the specifications of the Fairchild Mo Patents. ('481 patent, col. 2, lines 29-32 and 59-62; '406 patent, col. 2, lines 34-37 and 64-67.)

48. I understand that AOS contends the term “adjusted” means "selecting by repeated experiments or by computer simulation the relative depths of the well and the junction for the purpose

of moving initiation of breakdown in the device toward the center of the body region between adjacent trenches." I disagree with AOS's proposed construction. As discussed above, a person of ordinary skill in the art would apply the ordinary meaning of the claim language, and AOS's construction conflicts with that meaning. Specifically, AOS appears to construe "adjusted" to mean "selecting by repeated experiments or by computer simulation." A person of ordinary skill in the art would not understand the specifications of the Fairchild Mo Patents or their file histories to restrict the meaning of "adjusted" in this way. AOS further appears to construe "so that" to mean "for the purpose of." In other words, I understand that AOS's position is that the depth adjustment required by the claim language must be done with the intent of spacing the peak electric field or breakdown initiation point toward a specific location. Once again, there is nothing in the specifications or file histories which supports this interpretation. The language "so that" requires the adjustment achieve a particular result (e.g., the peak electric field being spaced away from the trench), not that the device designer have a specific goal in mind in making the adjustment. The usage of this term in the specifications is consistent with my interpretation. ('481 patent, col. 2, lines 29-32 and 59-62; '406 patent, col. 2, lines 34-37 and 64-67.) Finally, AOS appears to construe "spaced away from the trench" to mean "toward the center of the body region between adjacent trenches." A person of ordinary skill in the art would not interpret the claim language in the narrow way AOS proposes. The claim requires the peak electric field or breakdown initiation point to be located away from a location, i.e., spaced away from the trenches, not toward a location, as AOS urges. This fact follows naturally from the ordinary meaning of the claim language. In addition, the specifications of the Fairchild Mo Patents confirm my conclusion. They disclose essentially two different locations for the peak electric field or breakdown initiation point-- they can be spaced away from the trenches (e.g., '481 patent, col. 2, lines 29-32), or toward the halfway point between adjacent trenches (e.g., '481 patent, col. 5, lines 8-12.) A person of ordinary skill in the art would understand the claim language to cover the former embodiment, which is broader than the latter. Accordingly, AOS's proposed construction is incorrect.

ACTING AS A FIELD PLATE TO EXTEND THE DEVICE BREAKDOWN VOLTAGE IN THE TERMINATION REGION; FORMING A FIELD PLATE AROUND THE TERMINATION REGION

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
acting as a field plate to extend the device breakdown voltage in the termination region forming a field plate around the termination region	'947 Patent, claims 1, 5, and 6	acting as a conductive structure at or near the top surface of the substrate to increase breakdown voltage in the termination region forming a conductive structure at or near the top surface of the substrate that increases breakdown voltage in the termination region	a conductive ring formed in a trench in the termination region, resulting in a higher breakdown voltage in the termination region by modifying the depletion layer in the underlying silicon

49. Fairchild's proposed construction of "acting as a field plate …" and "forming a field plate …" is consistent with the understanding of a person of ordinary skill in the art. Such a person would understand that a field plate could be formed on the surface of the device, in a trench formed in the device, or partially on the surface and partially in a trench. Conventionally, field plates can be formed entirely within a trench within the device, entirely on the surface of the device, or partially in a trench and partially on the surface. These options are conveyed by Fairchild's proposed construction. Furthermore, the '947 Patent repeatedly states that the field plate affects device performance by increasing the breakdown voltage of the device. (E.g., '947 patent, col. 1, lines 34-39; col. 2, lines 37-40). Fairchild's construction correctly reflects this function of field plates.

50. I believe that AOS's proposed construction of this term is inconsistent with the understanding of a person of ordinary skill in the art. AOS's proposed construction requires that the structure forming, or acting as, a field plate must be a conductive ring that is "formed in a trench." AOS's proposed construction is unclear as to whether the "conductive ring" must be entirely or only at least partially within a trench. A person of ordinary skill in the art would understand that a field plate need not be formed entirely in a trench. Furthermore, there is no need to incorporate any language relating to a "trench" into the proposed construction of this term. The requirement in the '947 Patent claims that the field plate must be formed at least partially within a trench stems from other claim language.

51. Furthermore, AOS's proposed construction requires that the increase in breakdown voltage be caused by "modifying the depletion layer in the underlying silicon." In my opinion, it is not necessary to mention depletion layers in the construction of this term. There is nothing in the patent or its file history which requires this limitation. A depletion layer is simply a region within a semiconductor material that is devoid of free carriers (i.e., electrons or holes that facilitate the flow of electrical current). Any conductive structure in a semiconductor device that is in the vicinity of a junction can affect nearby depletion layers. Yet such structures are not defined by their tendency to affect the depletion layer. I see no reason why it is necessary to define a field plate by more than its actual structure and its effect on performance. Including a description of the effect on the depletion layer adds only confusion, rather than clarity, to the meaning of this term.

52. I have reviewed the portion of "Modern Power Devices," by B. Jayant Baliga, which AOS has cited in support of their proposed construction. I believe that AOS cites the Baliga textbook to support its argument that field plate must modify the depletion layers in the underlying silicon. In my opinion, however, the Baliga textbook does not support AOS's proposed construction. The '947 Patent cites the Baliga textbook at column 1, lines 43 to 52, as describing prior art edge termination designs. The pages of the Baliga textbook cited by AOS include a discussion of conventional planar field plates, in contrast to the field plate claimed in the '947 Patent which is at least partially within a trench. A planar field plate would give a constant voltage only along a horizontal surface, whereas a trenched field plate would give a constant voltage along only a vertical surface. This difference in he location of the constant voltage will affect the shape of the depletion region. The term "underlying" strongly suggests horizontally beneath the field plate. A trenched field plate, however, will affect depletion regions vertically alongside the field plate. Moreover, a field plate that is partially planer and partially trenched will affect depletions both beneath and alongside the field plate. Consequently, I believe that AOS's proposed construction is technically incorrect.

53. Finally, AOS's proposed construction requires that the underlying substrate must be silicon. While silicon is by far the most commonly used material, a person of ordinary skill in the art would understand that other semiconductor materials could be used. There is no requirement in the claim language, or in the '947 specification, that the semiconductor device be formed using a silicon

substrate.

A PLURALITY OF ELONGATED INNER RUNNERS EXTENDING IN THE SAME DIRECTION

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
a plurality of elongated inner runners extending in the same direction	'947 Patent, claim 6	conductive structures formed in trenches extending in the same direction across the active area of the device	multiple substantially parallel gate trenches filled with a conductive material extending in one direction across the active transistor region

54. A person of ordinary skill in the art would understand that the “inner runners” recited in this claim term consist of a conductive material formed in trenches that extend across the active region. Both Fairchild's and AOS's proposed constructions correctly reflect this. AOS's proposed construction, however requires that the trenches extend in "one direction." It is unclear whether AOS's proposed construction would include or exclude certain semiconductor devices having a "closed cell" design. A semiconductor device with a closed-cell configuration sometimes includes transistor cells arranged in a grid, having MOSFET cells that are bordered on all sides by trench walls. For example, the cells often are square or hexagonal in shape, as shown in Figures 3 and 4 above. A semiconductor device with an open-cell configuration, on the other hand, generally includes cells arranged in parallel stripes, having MOSFET cells that are bordered on only two sides by trench walls. In my opinion, the claim term covers both open cell and closed cell designs, as long as some of the runners extend across the active area of the device in the same direction. With regard to closed cell designs in particular, the inner runners extend across the active area, and are intersected by runners extending in a different direction. The runners extending in a different direction may or may not extend across the entire active area. But, the fact that there are other runners intersecting the elongated inner runners does not preclude the elongated inner runners from falling within the scope of this claim language. AOS's proposed construction appears to have the goal of excluding devices having one set of inner runners extending in one direction, and another set of inner runners extending in another direction. For this reason, I disagree with AOS's proposed construction.

ISOLATION TRENCH

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
isolation trench	'947 Patent, claim 1	an insulating structure, having a wall near the die edge, which electrically isolates the body region from the die edge	a valley filled with dielectric material surrounded by sidewalls in the periphery of a semiconductor substrate that can prevent leakage into the substrate

55. Fairchild's proposed construction states that an "isolation trench" is an insulating structure, includes a sidewall, and functions to electrically isolate the body region from the die edge. AOS's proposed construction, on the other hand, requires that the isolation trench be surrounded by sidewalls. AOS's proposed construction ignores the manufacturing processes that are used conventionally to form semiconductor devices. Typically, numerous identical semiconductor devices are formed on a large circular wafer. After the devices are formed, they are separated from each other by a process called "dicing" or "singulation," in which a saw is used to mechanically cut the wafer such that numerous, usually identical, semiconductor devices are formed. Often, isolation trenches are formed between adjacent devices on a wafer, and the singulation step cuts through the isolation region to form separate devices. Thus, one wall of the isolation trench is located on one device, and the other wall is located on another device. The singulation step does not eliminate the isolation trench, but rather results in isolation trenches being present in adjacent devices. Moreover, the isolation trenches still perform their function of electrical isolation, despite having been cut through the middle. A person of ordinary skill in the art would not view the singulation step as destroying the isolation trenches. Rather, a person of ordinary skill would know that the singulation step creates two isolation trenches, one in each side of the scribe line (i.e., the line at which the devices are singulated).

56. Furthermore, I disagree with the requirement in AOS's proposed construction that the isolation trench can " prevent leakage into the substrate." It is unclear to me what AOS's proposed language is intended to mean. From the perspective of one of ordinary skill, it is likely that AOS intended to mean that the isolation trench prevents leakage of electrical current between the source and the drain, but this is not clear from the language of AOS's construction. Fairchild's proposed construction, on the other hand, clearly states that the isolation trench "electrically isolates the body

region from the die edge." This language is clearly understandable to a person of ordinary skill in the art, and it correctly identifies the function of the isolation trench.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct to the best of my knowledge and belief.

Executed this 13th day of March, 2008, in Mountain View, California.

Richard A. Blanchard

Richard A. Blanchard, Ph. D.

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